

Q1- Answer the following questions (24 marks)  
a- fill the following missing information: (6 Marks)

Application	Hardware Requirements	Type of suggested Computing device
Commercial: inventory, payroll, web serving, e-commerce	Integer arithmetic High I/O	Workstations Desktops (PCs)
Scientific/numerical: weather prediction, molecular modeling	large memory floating point arithmetic	<b>Hard applications.</b>
Embedded: automobile engines, microwave, PDAs	lower power low cost interrupt driven	Cell phones Consumer electronics

b- Write the abbreviation of the following terms: (4 Marks)

Term	Abbreviation
ISA	Instruction set Architecture
NP	<del>Dynamic N</del> <b>Nedved processor.</b>
DRAM	<del>Dynamic Random Access</del> Random Access memory
ASIC	Application specific integrated circuits
GPU	Graphics processing unit.
GPP	General purpose processor
CISC	Complex Instruction set computer
RTN	<b>Register file transfer.</b>

c- Mention two bottlenecks of Von-Neumann Architectures: (6 marks)

1-

**Sequential execution.**

2-

**Separating of memory.**



d. What are the advantages of having different addressing mode? (6 marks)

1. An addressing mode is hardware support for a useful way of determining a memory address
2. Different addressing modes solve different HLL problems

Q2. Consider the following expression (26 marks)

$$A = X * Y - Z + (X * W) - Z$$

a. Evaluate the following expression using 0-address machine and 2 address machine  
Assuming that: X, Y, Z, W are stored in memory

0-address machine	Code size	Memory access	1 address machine	Code size	Memory access
push X					
push Y					
MUL					
push Z					
SUB					
push X					
push W					
sub					
Add					
push Z					
sub					
pop A					

b. Calculate: (12 marks + 6 marks)

- 1- instructions code size (in bits) needed to execute the expressions assuming that the machine has 16 registers, 64 instructions and memory space equal 0.5 Gbytes.

Opcode specifier = 6 bits Memory specifier = 29 bits Register specifier = 4 bits.



Q3) Answer the following Questions:

a- An instruction set has four instruction classes A, B, C, D with CPI A=3, B=4, C=5, D=2. Two codes were run and gave the following counts (24 Marks)

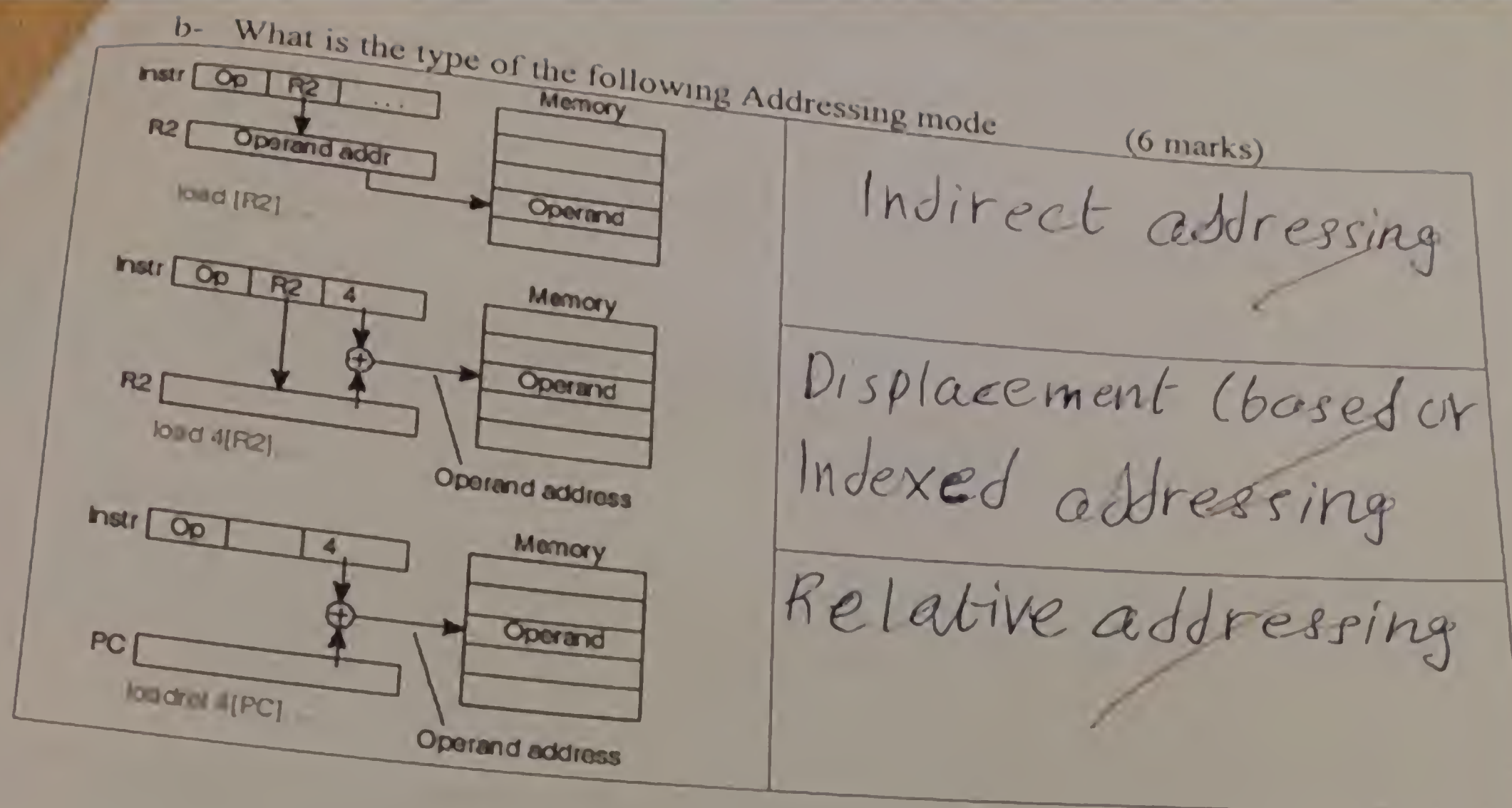
Code1: A=10, B=15, C=12, D=5 (18 Marks)

Code2: A=12, B=16, C=18, D=9

1- Calculate the execution time for Code 1 and code2 if the clock rate is 2Ghz

2- Calculate the MIPS rating for code 1 and code2





- Q4) Select the correct answer: (18 marks)
- 1- Which features are not found in RISC?
- ☒ a- Fixed format
  - ☒ b- Support big no of addressing mode
  - c- Load store architecture
  - d- None of the above
- 2- Full application Benchmarks are:
- ☒ a- Representative
  - ☒ b- Identify peak performance and potential bottlenecks
  - c- Easy to run, early in the design cycle
  - d- None of the above
- 3- Addressing mode is
- ☒ a- firmware support for a useful way of determining a memory address
  - b- software support for a useful way of determining a memory address
  - ☒ c- hardware support for a useful way of determining a memory address
  - d- None of the above
- 4- Which instruction is OK for load-store machine?
- a- add r1, r2, [0100]
  - ☒ b- st r1, [0100]
  - c- add a, b, c (a, b, c are in memory)
  - d- None of the above



- 5- Which of the following is a feature of a CISC machine?
- a- Instruction set work on operands only in registers
  - ☒ b- Fixed instruction format
  - c- The only way to access memory is by using load and Store instructions
  - ☒ d- None of the above
- 6- In indirect addressing mode:
- ☒ a- Instruction contains the operand
  - b- Instruction contains the address of the operand
  - ☒ c- Instruction contains the address of the address of the operand
  - d- None of the above
- 7- In relative addressing mode:
- a- Address of the operand = IR + constant
  - b- Address of the operand = register + constant
  - c- Address of the operand = constant
  - ☒ d- None of the above.
- 8- The motivation behind RISC architecture was:
- ☒ a- decrease the semantic gap between HLL and processor
  - b- Save memory space
  - c- Make pipelining easier
  - d- None of the above
- 9- Moor's law state that:
- ☒ a- The processor speed doubled every 1.5 year
  - b- The chip capacity doubled every 2 years
  - ☒ c- The memory capacity is doubled every year
  - d- None of the above
- 10- Scientific/numerical like molecular modeling needs:
- a- Integer arithmetic, high I/O
  - ☒ b- Large memory, floating-point arithmetic
  - c- Low power, low cost, interrupt driven
  - d- None of the above
- 11- Load store Machine is also called
- a- Register to memory machine
  - ☒ b- Register to register machine
  - c- Memory to memory machine
  - d- None of the above



12- Variable-length encoding is used in:

- a- RISC
- ✓ b- CISC
- c- Hybrid machine
- d- None of the above.



b- Answer with F of T:

(8 Marks)

- 1- Workstation is Low cost/power device ~~F~~ ✓
- 2- CISC is new architecture ~~F~~
- 3- Moore's law state that 2X transistors/Chip Every 2 years ~~F~~ ✓
- 4- ARM is a Microcontroller ~~T~~ ~~F~~ ✓
- 5- Microcontroller is used in smart phone ~~F~~ ✓
- 6- weather prediction needs integer arithmetic and high I/O operations ~~F~~ ✓
- 7- Simulator is less accurate than emulator in estimating system performance ~~T~~
- 8- RTN can produce a hardware design ~~T~~ ~~F~~